ABSTRACT OF THE DISCLOSURE

[0092] A field-programmable gate array (FPGA) comprising an array of RAM memory cells comprising at least one row of RAM memory cells, each RAM cell of the at least one row of RAM memory cells coupled to a row driver line; a row decoder coupled to a first end of the row driver line of each at least one row of RAM memory cells; a monitoring memory cell coupled to at least one of the row driver line; and where each monitoring memory cell is also coupled to a memory writing line. A method for an FPGA having a plurality of RAM memory cells as the programming mechanism, the FPGA further having erase circuitry for clearing the RAM memory cells for reprogramming of the FPGA. The method comprises providing at least one monitoring memory cell coupled to the erase circuitry; initiating a memory clear phase on at least one monitoring memory cell; and making a determination as to whether the output signal from each at least one monitoring memory cell indicates a cleared monitoring memory cell. The method may further comprise an act of writing to the at least one monitoring memory cell and a query of determining whether all of the at least one monitoring cell was properly written to.